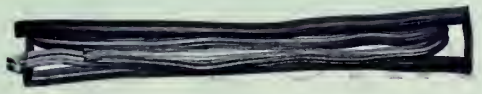
NONLINEAR COMPUTER MODELS OF FIELD-EFFECT TRANSISTORS

by

Arthur David Rathjen



United States
Naval Postgraduate School

THESIS

NONLINEAR COMPUTER MODELS
OF
FIELD-EFFECT TRANSISTORS

by

Arthur David Rathjen

June 1970

Nonlinear Computer Models of Field-Effect Transistors

by

Arthur David Rathjen
Lieutenant Commander, United States Navy
B.S., Illinois Institute of Technology, 1962

Submitted in partial fulfillment of the
requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

from the

NAVAL POSTGRADUATE SCHOOL
June 1970

ABSTRACT

Whenever active devices are included in an electronic circuit that is to be analyzed by a compter, appropriate models for these devices must be developed. A lumped large-signal dynamic model of the field-effect transistor (FET) is presented and the procedure for pointwise linearization of this model is described. This linearized model is suitable for use with the TRAC (Transient Radiation Analysis by Computer program) network analysis program. Implementation of this model using TRAC coding was demonstrated by programming an example circuit for each of two basic types of field-effect transistor. The performance of the model in simulating a basic pulse invertor circuit was compared with actual device behavior. Suggestions for extension of this work are included.

TABLE OF CONTENTS

I. INTRODUCTION

When a computer is used to analyze an electronic circuit, the user, through the input routine of the analysis program, must provide sufficient information concerning the circuit parameters and device terminal relationships to allow the network equations describing the circuit to be determined and solved. This is a simple task for passive linear components such as resistors, capacitors, and inductors; but active nonlinear devices must be described to the computer analysis program in terms of mathematical models which simulate the behavior of the device. As field-effect transistors (FETs) have become more common in electronic circuits, it has become increasingly important to develop accurate models of these devices for use in computer programs used in design and analysis of such circuits.

Small-signal FET models are easily produced for any analysis program which includes voltage-controlled current or voltage sources as allowable circuit elements. Any modern basic electronics textbook [1] includes a description of such models. These are valid only over a small range near the bias point at which the parameters were determined. Large-signal models, which are valid over the entire operating range of the device, are required for dynamic analysis of logic and switching circuits, for very accurate analysis of large-signal "linear" circuits (such as various classes of amplifiers, limiters, and mixers), and for special circuits in which the FET is used as a voltage-controlled current source or as a voltage-variable resistor.

Today's circuit designer can choose from many computer-aided design (CAD) programs which offer a great variety of features including frequency response, time response, transfer functions, and pole and zero locations; but all general-purpose and most special-purpose analysis programs include the basic time-response solution of the network equations. ECAP [2] and TRAC [3] are two such programs. ECAP is a widely used general-purpose analysis program with time-response output only. TRAC is the network analysis program which was used in developing the FET models presented in this paper.

Roberts and Harbourt [4] developed piecewise linear large-signal FET models for use with ECAP. ECAP requires that active devices be represented by linear passive elements and controlled current sources. Branch current-sensing switches are used to change parameter values when going from one piecewise linear section to another. ECAP large-signal modeling is thus inconvenient, requiring the introduction of switches and additional network nodes and elements to generate the piecewise approximation to the nonlinear FET characteristics. These detract from the total network node and element capability of ECAP.

The TRAC program is much more flexible and allows the analyst to define his own models by writing a FORTRAN subprogram in which he enters terms directly into elements of the network matrix equations. This paper describes the development of nonlinear models for FETs and the procedure for determining the matrix terms using an iterative pointwise linearization of the nonlinear FET characteristics.

The discussion here is given in terms of n-channel devices although FETs of all types are also made with p-type channels which operate in

the same fashion with current directions and all voltage polarities reversed. Inclusion of these complimentary types would have complicated the discussion without demonstrating anything new or different.

II. BACKGROUND

A. FIELD-EFFECT TRANSISTOR CHARACTERISTICS

The theory of operation, advantages of using, and techniques of manufacturing field-effect transistors (FETs) have been well described elsewhere and only an introductory review of their operating characteristics is necessary for understanding the computer model of these devices. Extensive bibliographies of FET studies [5,6,7] have been produced to guide researchers who require more detailed information about the devices.

An FET is basically a piece of lightly doped semiconductor material in which the size and shape of the conducting portion, called the channel, is modulated by a controlling voltage to produce variable conductance. The terminal to which the control voltage with respect to the channel is applied is called the gate. A salient feature is the pinch-off characteristic, in which the channel saturation current is limited to a level determined by the controlling gate voltage.

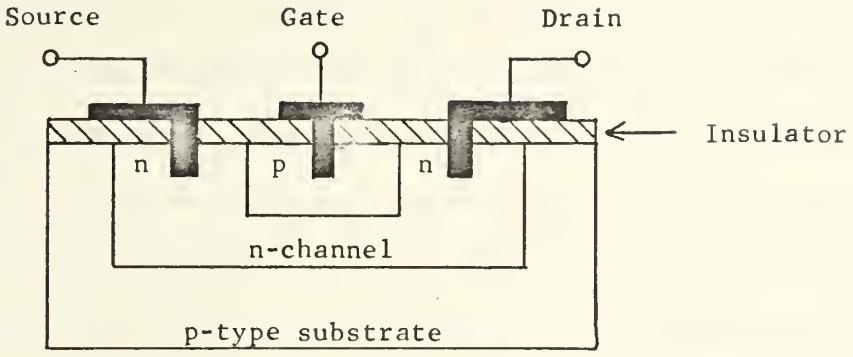
The channel current is carried by majority carriers under the influence of an applied electric field. Mobile carriers travel from the end of the channel called the source, to the opposite end, the drain, to which the attracting electric field is applied. Many FETs are symmetrical, i.e., the source and drain ends of the channel are interchangeable.

In the junction field-effect transistor (JFET), channel modulation is accomplished by depleting its carriers by reverse-biasing of the P-N gate-channel junction. This restricts operation of this type to the

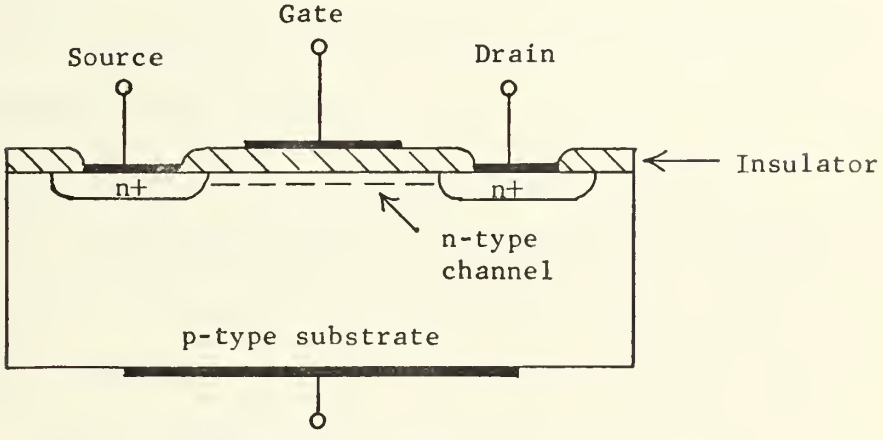
polarity which provides this reverse bias. Since the channel is lightly doped and the gate diffusion region is more heavily doped, small reverse voltages on the gate are capable of depleting a large portion of the channel.

Insulated-gate field-effect transistors (IGFETs) are surface-controlled devices and channel modulation depends on a modification of the charge distribution when an electric field is applied to the surface. This field is obtained by applying a voltage to an electrode (the gate) which is a thin metal film deposited on a solid dielectric material insulating it from the channel. The metal is commonly aluminum and the insulator is usually an oxide such as silicon dioxide (SiO_2). For this reason IGFETs are also called MISFETs, for metal-insulator-semiconductor FET, and the primary subgroup which uses an oxide insulator is called MOSFET, to describe the metal-oxide-semiconductor structure.

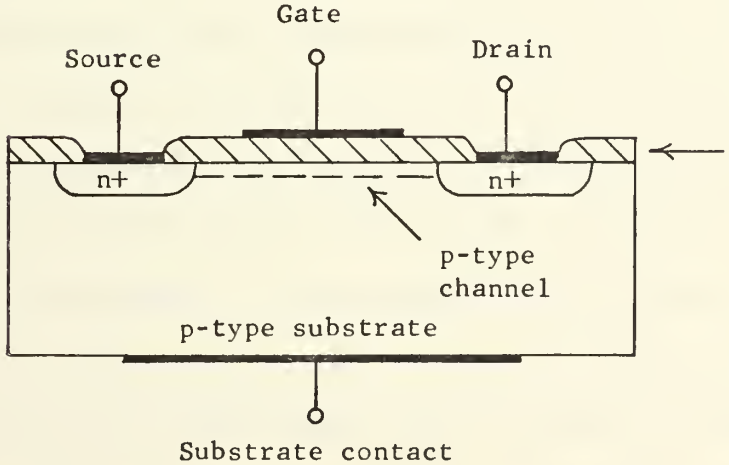
The channel under the insulated gate is very lightly doped and it is possible to apply a field large enough to invert the doping concentration. This is used to produce two different types of IGFET. If the drain and source contacts are made at regions in which n-type material has been diffused, a depletion-enhancement type IGFET, often called simply a depletion type, can be made by connecting these two regions with a lightly doped n-type channel. By immobilizing charge carriers, a negative voltage applied to the gate depletes the channel of usable carriers. If the field is high enough, the channel can become intristic and inverted to p-type, completely cutting off channel current. If a positive voltage is applied to this gate, electrons will be attracted into the channel, enhancing its conductivity. Thus this type is capable of operating with either polarity of voltage on the controlling gate.



(a)



(b)



(c)

Figure 1. Field-effect transistor structures: (a) Junction FET, (b) Depletion-type IGFET, (c) Enhancement-type IGFET.

The third type of FET is the enhancement IGFET. If the drain and source n-type regions are diffused into a very lightly p-doped channel, conduction will not take place until the channel is inverted by applying sufficient positive voltage to the gate. The voltage at which conduction begins is called the threshold voltage, V_T. Production of enhancement-type IGFETs requires very light doping of extremely pure semiconductor material. Manufacturers are making efforts to reduce the magnitude of V_T as much as possible.

Simplified structure diagrams of these three types of field-effect transistors are shown in figure 1.

The IGFET channel is laid out on a lightly doped substrate of opposite doping type. In normal operation the substrate is connected to the source, but often the substrate lead is brought out separately and a bias voltage or signal may be applied, making the IGFET a four-terminal device. Long [8] found that for several transistor types at a variety of values of terminal voltage, channel current was nearly independent of the substrate bias voltage, V_{SS}. He reported that the only noticeable effect was (for an enhancement type device) a few tenths of a volt variation in V_T for a zero to 20 volt variation in V_{SS}.

Of interest to the circuit analyst are the terminal I-V relationships and immitance characteristics of the device. Since the IGFET channel current is independent or only weakly dependent on the substrate voltage, and since in most applications the substrate and source are interconnected, the three types of FETs can be considered as three-terminal devices. Dual-gate MOSFETs are true four-terminal devices in that channel current is strongly dependent upon all four terminal

voltages. Particular device characteristics are dependent upon geometrical structure and placement of the two gate electrodes.

Early derivations of FET characteristics started by considering the impurity profile of the channel and gate-channel contact. This led to solutions valid only for the particular doping profile under consideration. Sevin [9] showed that although different profiles led to expressions of different form, all profiles, including the extreme cases, gave approximately the same numerical result. Sevin was thus able to choose a profile which gave a simple expression for the square-law transfer characteristic. Middlebrook's charge-control approach [10] resulted in a simplified derivation valid for all types of FETs and gave the same simple expression shown by Sevin. Based on this work, Angelo [1] has set forth a set of equations describing the functional dependence of channel current on the drain, source, and gate voltages, v_D, v_S, and v_G respectively. These have been used here. Single-gate FETs have two primary operating regions, the triode region in which the device behaves as a voltage-variable resistor, and the pinchoff (or pentode) region where the current is determined mainly by the gate voltage. The boundary between these regions is the locus of points where the gate and drain-to-source voltages combine to just pinch off the channel, resulting in saturation.

In the triode region, $0 < v_{DS} < v_{GS} - V_P$,

$$i_{DS} = \frac{I_{DSS}}{V_P^2} \left[2(v_{GS} - V_P)\, v_{DS} - v_{DS}^2\right] \qquad (1)$$

where V_P is the pinch-off voltage (that voltage which when applied to the gate, is alone sufficient to pinch off the channel) and where I_{DSS} is a

constant (the drain saturation current) which depends upon channel geometry, impurity density and profile, and charge carrier mobility (and hence temperature). I_{DSS} is defined to be the channel current, i_{DS}, at $v_{GS} = 0$ and $v_{DS} = -V_P$.

In the pinch-off region, $0 < v_{GS} - V_P < v_{DS}$,

$$i_{DS} = I_{DSS} \left(1 - \frac{v_{GS}}{V_P}\right)^2 . \qquad (2)$$

Here, for an ideal device, the current is independent of v_{DS}, for $v_{DS} > v_{GS} - V_P$. In an actual device there is a small channel conductance, g_{dp}, in the pinch-off region, which varies with v_{GS} in such a way as to always be small compared to the transconductance effect.

Equations 1 and 2 are valid for junction FETs and depletion-type IGFETs. For $1 < v_{GS}/V_P$ the channel current is essentially zero. The JFET is restricted to operation with the gate biased so as to reverse-bias the P-N junction. Although a forward bias destroys the junction, transient forward voltages of a few tenths of a volt are permitted and equations 1 and 2 apply.

The enhancement-type MOSFET has a characteristic threshold voltage, V_T, instead of the pinchoff voltage V_P, but the equations are of the same general form:

$$\text{for } 1 < v_{GS}/V_T , \qquad i_{DS} = 0 \qquad (3)$$

and for an n-channel device, for $0 < v_{DS} < v_{GS} - V_T$, (triode region)

$$i_{DS} = K(2(v_{GS} - V_T)\, v_{DS} - v_{DS}^2) \qquad (4)$$

and for $0 < v_{GS} - V_T < v_{DS}$ (pinch-off region)

$$i_{DS} = K(v_{GS} - V_T)^2 . \qquad (5)$$

Here K is a constant not equal to I_{DSS}/V_T^2 since I_{DSS} has no meaning in the enhancement type device where $i_{DS} = 0$ when $v_{GS} = 0$. K is a function of channel geometry, doping, and effective carrier mobility.

B. THE TRAC NETWORK ANALYSIS PROGRAM

1. General

TRAC (Transient Radiation Analysis by Computer) is a digital computer program which simulates the time response of an electronic circuit to one or more arbitrary forcing functions. It is a special-purpose program in that these forcing functions may be radiation stimuli as well as electrical inputs. An extremely flexible program, it is suitable for general network analysis in or out of a radiation environment, and has features which make it especially suitable for modelling of nonlinear devices and components.

TRAC is capable of initializing and computing the time solution of a large general set of simultaneous linear and nonlinear, ordinary integral and differential equations, provided the user puts these into a finite defference equation of specified form.

The version of TRAC available for this study was written in FORTRAN IV and assembly language adapted for use on the IBM-360/67. This version used 158 k bytes of storage. Information given here about the TRAC program should be sufficient for understanding the non-standard modelling procedure used here. Those who require detailed information will find TRAC to be well documented in references 3 and 11.

TRAC uses the nodal analysis method which permits topological circuit description and data entry. TRAC has built-in models for linear circuit elements (resistors, capacitors, and inductors), current and

voltage sources, diodes, and bipolar junction transistors (BJTs). It also has a routine to automatically write the nodal equations for the network using these built-in models with topological input data, and solves these equations for the node voltages. TRAC also calculates branch currents and powers.

In TRAC analysis, a network is treated as a set of nodes interconnected by network elements as shown in figure 2. The reference (ground) node and other independent nodes are not unknown and are not included in the analysis. The current $i_{P,k}(t)$ is defined to be the current leaving the P^{th} node due to the voltage-current (I-V) constraints on the k^{th} network element and the unknown node voltages, at time t. This current has a functional relationship to the node voltage, the parameters of the network elements, the current and voltage sources, and time, t:

$$i_{P,k}(t) = F_{P,k}(\underline{v},\rho,\underline{e},\underline{i},t) \qquad (6)$$

The exact form of this function depends on the network topology and the I-V relationship of the k^{th} element.

By Kirchhoff's current law (KCL), the total current leaving each node is zero, since no charge is stored at the node; therefore

$$\sum_k i_{P,k}(t) = 0 \quad , \quad \text{for each node P} \quad . \qquad (7)$$

In TRAC, the I-V relationship affecting the current leaving node P for the k^{th} element is represented by a linear difference equation which can be put into the form

$$i_{P,k}(t_n) = \left[\sum_Q \Delta h_{P,Q,k}(t_n) \cdot v_Q(t_n) \right] - \Delta w_{P,k}(t_n) \qquad (8)$$

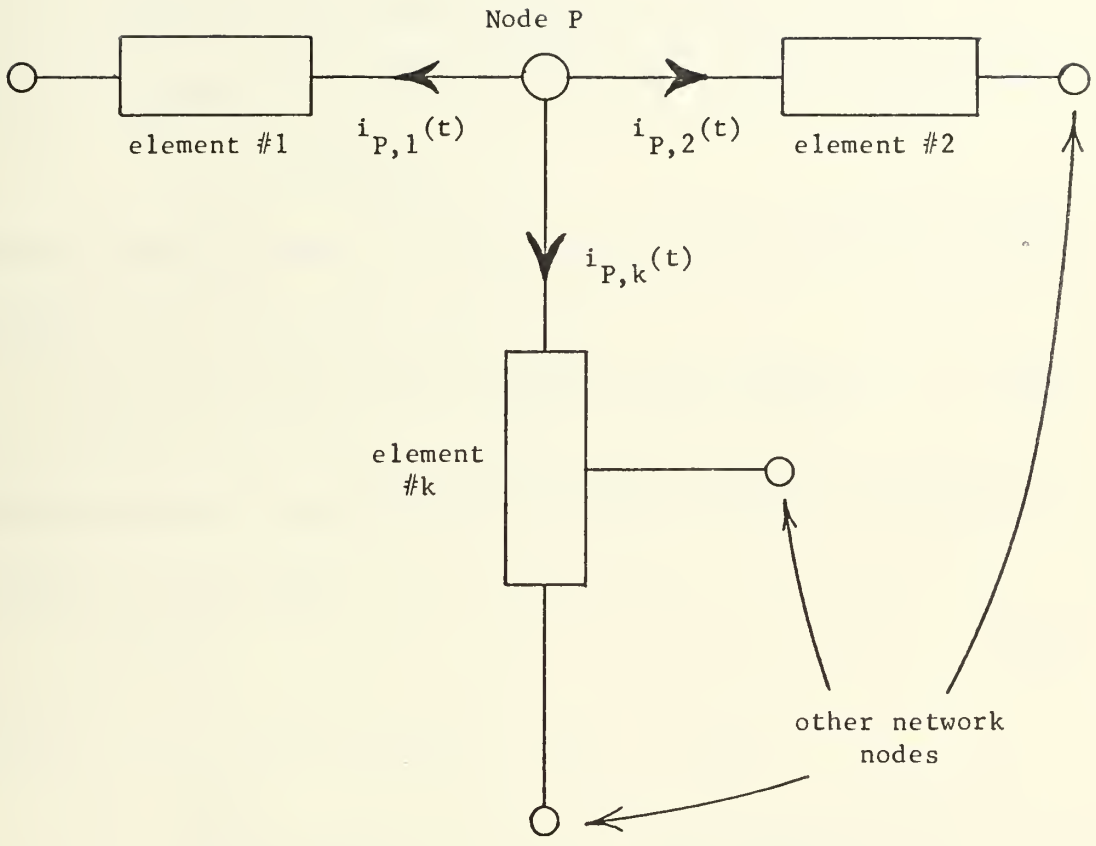


Figure 2. TRAC concept of a set of nodes interconnected by network elements.

where P and Q are node numbers,

$\Delta h_{P,Q,k}(t_n)$ is the k^{th} network element admittance contribution at time t_n,

$v_Q(t_n)$ is the voltage of node Q at time t_n, and

$\Delta w_{P,k}(t_n)$ is the k^{th} network element current contribution at time t_n.

Substituting the current form of equation 8 into equation 7, yields another form of Kirchoff's current law:

$$\sum_k \left\{ \left[\sum_Q \Delta h_{P,Q,k}(t_n) \cdot v_Q(t_n) \right] - \Delta w_{P,k}(t_n) \right\} \equiv 0 \qquad (9)$$

Writing equation 9 simultaneously for each node P, in the network, yields the matrix form:

$$H \cdot V = T \qquad (10)$$

where V is the vector $[v_1, v_2, \ldots v_Q, \ldots v_{NV}]^T$,

$$H = \begin{bmatrix} \sum_k \Delta h_{1,1,k}(t_n) & \cdots & \sum_k \Delta h_{1,NV,k}(t_n) \\ \vdots & & \vdots \\ \sum_k \Delta h_{NV,1,k}(t_n) & \cdots & \sum_k \Delta h_{NV,NV,k}(t_n) \end{bmatrix},$$

$$T = \left[\sum_k \Delta w_{1,k}(t_n) \quad \cdots \quad \sum_k \Delta w_{NV,k}(t_n) \right]^T$$

and NV is the number of dependent nodes.

The nodal admittance matrix, H, is normally nonsingular and is a sparse matrix. Diagonal terms represent element conductances; off-diagonal terms occur symmetrically and represent transconductances.

TRAC proceedes to solve the matrix equation 10 repeatedly, using automatic time step (Δt) control. An automatic DC initialization is only a special case of the transient solution. In the version of TRAC available for this study, equation 10 was solved using Gaussian elimination with pivoting although the sparseness of the matrix indicates a more computationally efficient method could have been used.

2. Nonlinear Modelling Procedure

TRAC handles the nonlinearity of the diode primary diffusion current equation, which is an exponential function, by pointwise linearization and a modified Newton-Raphson iteration scheme [11]. Using this standard diode model, a modified Ebers-Moll transistor model for a BJT is constructed using two diode standard models and two controlled current sources. TRAC has a capacity for thirty of these diode or transistor models to be used in any network. The TRAC User's Guide, reference 3, describes how models can be constructed for zener diodes, unijunction transistors (UJTs), silicon control rectifiers (SCRs), and four-layer PNPN switches. These non-standard models are combinations of the TRAC built-in diode, transistor, and linear element models. It is significant that no such model is suggested for any type of field-effect transistor.

Any mathematical model of any field-effect transistor must involve a square-law transfer function rather than the exponential function characteristic of the diffusion current devices. Thus the only nonlinear equation built into TRAC is inappropriate for modelling of field-effect transistors, and no combination of the TRAC standard built-in models will suffice.

The TRAC program achieves its remarkable flexibility by calling a user-written FORTRAN language subroutine in which the user has access to nearly all the program variables during program execution at four separate times during each iteration. This is where the user can enter any function (such as the square-law transfer function for the FET) and the statements for calculating and entering terms directly into the network matrix equations. The equations describing the mathematical model must be written as linear difference equations of the form of equation 8. The Δh and Δw terms are then computed and entered directly.

III. FIELD-EFFECT TRANSISTOR MODELS

A. GENERAL

A good model must posses two important attributes: it must accurately simulate the device characteristics over the range of intended use, and it must be computationally efficient. It is also desireable that required device parameters be economical to obtain, either provided on the manufacturer's specification sheet or easily measured.

The pointwise linearization method employed here generates a linear small-signal model at each step in the time solution. Of course it is not economical to measure device characteristics at each of the possible operating points, nor would storage and retrieval of these parameters lend itself to computational efficiency. The parameters appropriate to each point are better determined by partial differentiation of the device I-V expressions and evaluation of these derivatives at that point. If the functions involved are continuous and accurately express device behavior, a simple iterative scheme can be devised and convergence criteria chosen to give a very high degree of accuracy at all points.

Equations 1 and 2 express the I-V relationships for junction FETs and depletion-type IGFETs. These equations have the advantage of being equal at the locus of points $v_{DS} = v_{GS} - V_P$, which describes the boundary between the triode and pinch-off operating regions. The slopes of these two equations are both equal to zero at this boundary for an ideal device.

B. TRIODE REGION ANALYSIS

1. Pointwise Linearization

In the triode region, $0 < v_{DS} < v_{GS} - V_P$, partial differentiation of equation 1 gives

$$g_{DS} \equiv \left.\frac{\partial i_{DS}}{\partial v_{DS}}\right|_{v_{GS}=VGS} = \frac{I_{DSS}}{V_P^2}\left[2(VGS - V_P) - 2v_{DS}\right] \qquad (11)$$

At an arbitrary point (VDS, IDS) on the output characteristics curves, figure 3, the pointwise linear approximation to the output curve is the straight line

$$i_{DS} = GDS\ (v_{DS} - VDS) + IDS \qquad (12)$$

where GDS is the slope at (VDS, IDS) given by

$$GDS = g_{DS}\Big|_{(VDS,\ VGS)} = \frac{I_{DSS}}{V_P^2}\left[2(VGS - V_P) - 2\ VDS\right] \qquad (13)$$

Use of FORTRAN notation for TRAC variables from this point is more convenient and adds clarity. In TRAC notation, the array terms are denoted by

$$\Delta h_{P,Q,k}(t_n) \equiv H(P,\ Q) \quad \text{and}$$

$$\Delta w_{P,k}(t_n) \equiv T(P) \quad .$$

Putting equation 12 into the form of equation 8 and using FORTRAN notation for the variables, gives

$$i_{DS} = (GDS)\ v_D\ (t_n) + (-GDS)\ v_S\ (t_n) - (GDS\ *\ VDS - IDS)$$

Since $i_{D,k}(t_n) = i_{DS}(t_n)$ and $i_{S,k}(t_n) = -i_{DS}(t_n)$,

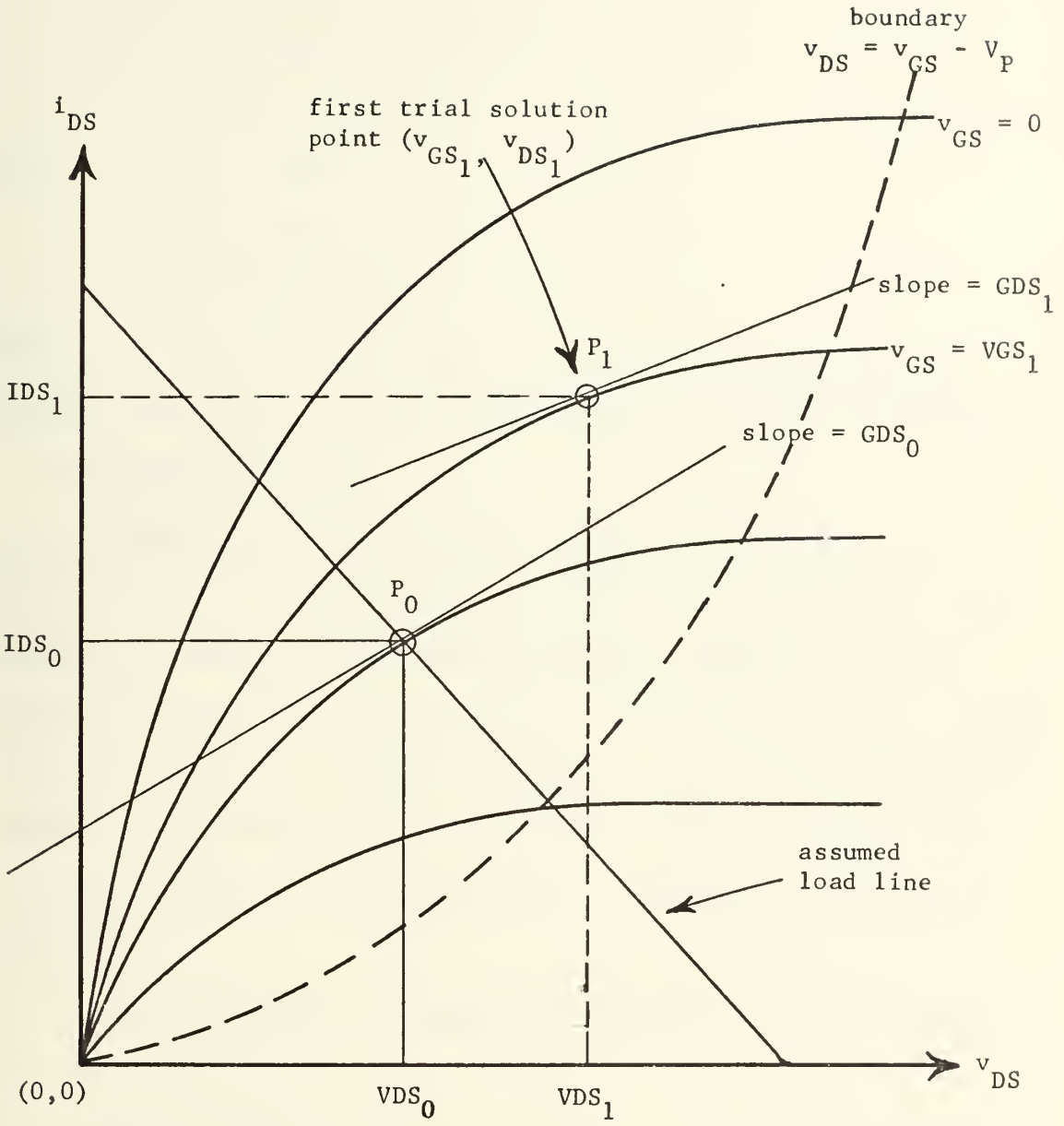


Figure 3. Triode region convergence procedure showing one iteration from initial point P_0 to the first trial solution point, P_1.

H(D, D) = GDS

H(D, S) = -GDS

T(D) = GDS * VDS - IDS

and H(S, D) = -GDS

H(S, S) = GDS

T(S) = IDS - GDS * VDS

where D and S are the network node numbers to which the drain and source, respectively, of the k^{th} field-effect transistor are connected.

2. Convergence Method

Choice of the starting point, (VDS_0, IDS_0) in figure 3 is arbitrary but the TRAC DC initialization program begins with all node voltages set equal to zero. During the time solution it is both logical and convenient to start each new time step t_n using the voltages $V(t_{n-1})$ calculated at the previous time, t_{n-1}, at which a solution was accepted. These voltages are automatically updated by TRAC each time a new time solution is accepted and time is advanced by the current value of Δt.

For each iteration within a time step, VGS and VDS are given by

$$VGS = v_G - v_S \tag{14}$$

and

$$VDS = v_D - v_S \tag{15}$$

where v_G, v_D, and v_S are the current, or trial solution values, of the FET terminal voltages. GDS is given by equation 13. Then let

$$IDS = \frac{I_{DSS}}{V_P^2} \left[2(VGS - V_P)\, VDS - (VDS)^2 \right] \tag{16}$$

Using these values, the matrix terms described above are then entered and the network matrix equation, equation 10, is solved for a trial solution,

$$V = [v_1, v_2, \ldots, v_D, v_S, v_G, \ldots, v_{NV}]^T \qquad (17)$$

The load line shown in figure 3 represents the linearization of the I-V relationship of the equivalent circuit of the external network looking in at the nodes to which the source and drain are connected. The only thing known about this line is that if the point (VDS, IDS) satisfies the network matrix equation, then this load line will pass through (VDS, IDS). In any case, this load line will pass through the first trial solution point, (VDS_1, IDS_1), which is determined by substituting the trial solution into equations 15 and 16. This represents a return to the output curve for $v_{GS} = VGS_1$ along a line of constant voltage, VDS_1. This new point is used to calculate (VDS_2, IDS_2), the next iteration, by the same procedure. This process is iterated until the convergence criteria,

$$|VDS - v_D + v_S| \leq \delta \quad \text{and}$$

$$|VGS - v_G + v_S| \leq \delta$$

are satisfied, where δ is a small, arbitrary constant. At this time the trial solution is accepted, and the TRAC program updates the program variables and time is incremented by Δt to t_{n+1}. The above procedure is then repeated for this next time step.

C. PINCH-OFF REGION ANALYSIS

1. Pointwise Linearization

In the pinch-off region, $0 < v_{GS} - V_P < v_{DS}$, i_{DS} for an ideal device is given by equation 2. In an actual FET, i_{DS} in the pinch-off region is not completely independent of v_{DS}. The magnitude of this effect depends on the design of the transistor. The gradual increase in i_{DS} with increasing v_{DS} is partly due to the fact that channel length does not remain constant under pinch-off conditions as was assumed in the theoretical analysis leading to equation 2, but decreases slightly with increased voltage. This has a greater effect in short-channel devices designed for high-frequency applications. It can be neglected in audio FETs. This non-zero slope, g_d, can easily be measured at any bias point, and for a small-signal model, incremental drain current is given by

$$i_{ds} = g_m v_{gs} + g_d v_{ds} .$$

For large-signal modelling by pointwise linearization, the functional relationship $i_{DS} = f(v_{GS}, v_{DS})$, must be known in analytic form. The partial derivative $\partial i_{DS}/\partial v_{DS}$ can then be evaluated exactly as it was in the triode region case. This functional relationship is not known in general but can be approximated empirically for a given device by measurements, if the desired degree of accuracy so requires.

Since in equation 2 i_{DS} is independent of V_{DS}, g_{DS} is zero, and we let

$$g_m \equiv \frac{\partial i_{DS}}{\partial v_{GS}} = - \frac{2I_{DSS}}{V_P} \left[1 - \frac{v_{GS}}{V_P} \right] . \qquad (18)$$

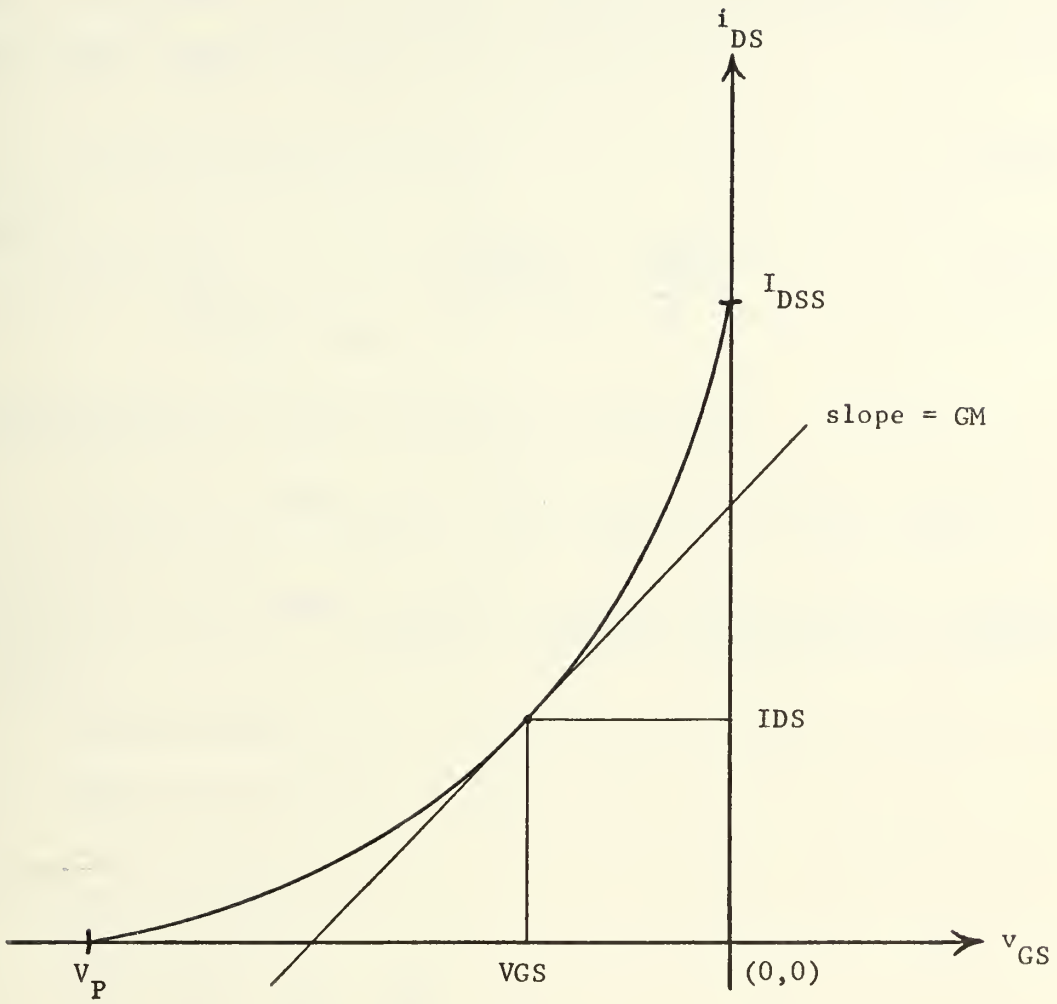


Figure 4. Pinch-off region transfer curve showing pointwise linearization procedure.

This is the slope of the transfer characteristic curve, figure 4. At a point (VGS, IDS) the tangent line is given by

$$i_{DS} = GM\ (v_{GS} - VGS)\ IDS \tag{19}$$

where

$$GM = g_m\Big|_{v_{GS} = VGS} = -\frac{2I_{DSS}}{V_P}\left[1 - \frac{VGS}{V_P}\right] . \tag{20}$$

Putting equation 19 into the form of equation 8,

$$i_{DS}(t_n) = (GM)\ v_G(t_n) + (-GM)\ v_S(t_n) - (GM * VGS - IDS) .$$

As in the triode region, $i_{D,k}(t_n) = i_{DS}(t_n)$ and $i_{S,k}(t_n) = - i_{DS}(t_n)$. Therefore

H(D, G) = GM

H(D, S) = -GM

H(S, G) = -GM

H(S, S) = GM

T(D) = GM * VGS - IDS

T(S) = -GM * VGS + IDS

where D, S, and G are the network node numbers to which the drain, source, and gate, respectively, of the k^{th} FET, are connected.

2. Convergence Method

Convergence is achieved in the pinch-off region by the same method employed in the triode region. For each iteration within the time step, t_n,

$$VGS = v_G - v_S . \tag{21}$$

and GM is calculated by evaluation of equation 20. Then IDS is given by

$$IDS = I_{DSS} \left[1 - \frac{VGS}{V_P}\right]^2 \quad . \tag{22}$$

Starting at this point, (VGS, IDS), the above values are used to determine the matrix terms in equation 10 which is solved for a trial solution,

$$V = [v_1, v_2, \ldots, v_D, v_S, v_G, \ldots, v_{NV}]^T \quad .$$

The trial solution value v_{GS} is compared with the value of VGS to determine if convergence has been achieved, in which case the solution is accepted and program variables updated and time incremented. If convergence is not achieved, the solution proceeds back to equation 21 using the trial solution values to determine the next point (VGS_1, IDS_1) and a new value for GM.

D. LUMPED-PARAMETER MODELS

1. General

A physical device such as an FET operates by propagation of fields and movement of charge carriers between points in space. This propagation and motion takes time which results in delays in transmission of information between the device terminals. The interaction of fields and charge carriers in an FET is distributed throughout the entire active channel under the gate. Thus exact simulation of the behavior of this device requires a model in which both time and space variables are included. The models described in this section do not provide time delay and lumped analysis is used.

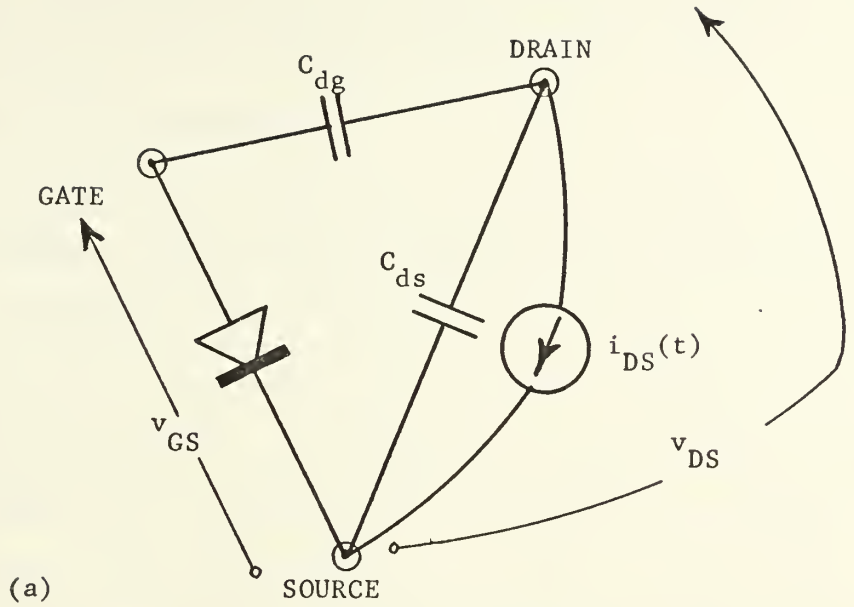
Reference 12 describes a distributed IGFET model and an associated computer program which includes space variables as well as

time to simulate IGFET behavior to high precision. This model is valuable for analysis of extrinsic effects and as an aid to design by prediction of the characteristics of proposed FET designs. This type of analysis model is incompatable with available second-generation network analysis programs since these programs require that distributed effects be lumped into discrete network elements.

In figure 1 it can be seen that the active channel under the gate in each of the three types of FET has a voltage drop distributed along its entire length. Thus voltage-dependent capacitance and leakage effects are distributed and continuously variable along the gate-to-channel interface.

2. Junction FET Model

Consider how the JFET gate appears to an external circuit. The channel depletion effect is distributed along the length of the gate P-N junction. This junction is reverse-biased and appears as a distributed capacitance with a high shunt resistance. The device control voltage is that which appears across this capacitance and is not necessarily equal to the input voltage due to the time required to discharge or charge this capacitance through the gate bulk semiconductor resistance. This capacitance must be split between the drain end of the channel and the source end to get the required lumped model. It is not equally distributed since the drain and the source are biased differently with respect to the gate in normal operation. The portion of the junction near the drain end of the channel is normally strongly reverse-biased and the capacitance value here is nearly independent of



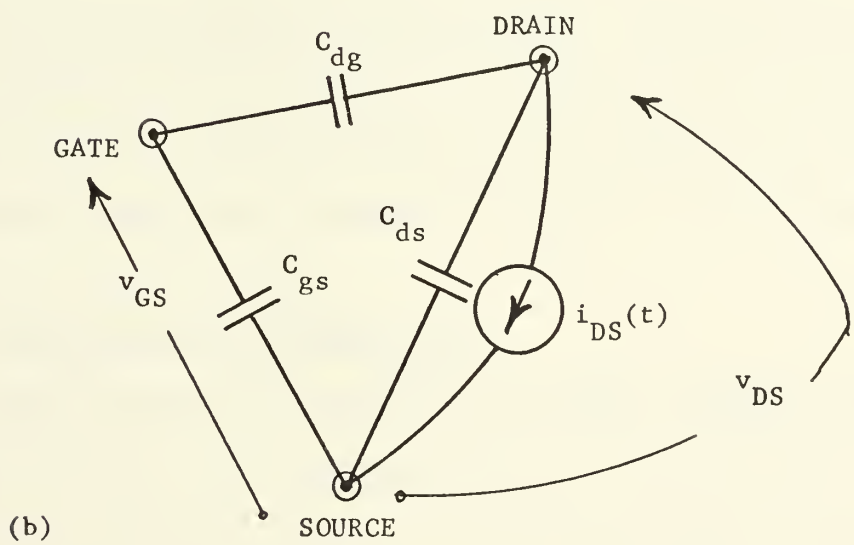


Figure 5. Lumped field-effect transistor models. (a) Junction FET, (b) Insulated-gate FET.

v_{GS}. This capacitance and the associated shunt conductance can be modelled using the TRAC standard capacitor model which includes provision for a shunt resistor.

The source end of the junction is less strongly reverse-biased or even slightly forward-biased, depending on the instantaneous value of v_{GS}. It exhibits the voltage-variable capacitance and conductance properties of an ordinary P-N junction diode. A lumped model of this gate-to-source junction can be produced by using the TRAC standard built-in model for a junction diode to simulate these effects.

These lumped approximations are shown in figure 5(a). The drain-source circuit has no current paths to the gate except for the leakage and capacitve effects mentioned above. Transconductance and output conductance are simulated by the nonlinear current source, i_{DS}, which is modelled by pointwise linearization as described earlier. The drain circuit capacitance is lumped into C_{ds} and is represented by the TRAC standard capacitor model.

3. Insulated-Gate FET Lumped Model

Figure 1 shows that the gate of an IGFET resembles a parallel-plate capacitor with a thin dielectric layer. The dielectric results in a very low gate conductance, and since the thickness is constant, the distributed capacitance is uniform along the channel and independent of v_{GS}. This capacitance can be split between the source and drain ends of the channel and both lumped capacitors simulated by the TRAC standard capacitor model. This approximation is shown in figure 5(b). This model can be used for both depletion-type and enhancement-type IGFETs, the only difference being in the expressions used to obtain the linearization of i_{DS}. Equations 4 and 5 which are applicable to the

enhancement-type IGFET are of the same form as equations 1 and 2 respectively, for the depletion-type IGFET. Thus the pointwise linearization and iteration process for convergence is the same for both types of IGFET.

IV. EXPERIMENTAL RESULTS

A. PARAMETER DETERMINATION

1. General

Accurate simulation of FET circuits requires not only a model of suitable form but also accurate parameter data to be used with the model. It would be ideal if the required information could be obtained from the manufacturer's specification sheet for a particular device. With present fabrication techniques useable FETs of a particular type are produced with a wide spread of parameter values; to demand close tolerances would result in low yields. Therefore specification sheets list a range or "typical" parameter value, and where a particular parameter is critical to some aspect of performance, a maximum or minimum value is listed. This insures that any given device of that type will meet certain minimum performance criteria although many will exceed them.

Often the circuit being analysed must be insensitive to parameter variations and must perform satisfactorily under worse-case conditions. In such a case, the maximum, minimum and typical values given on the specification sheet can be used as a starting point for worst-case and sensitivity analysis. In other cases the circuit to be simulated will be one in which the circuit is to be carefully adjusted for optimum performance with a particular device installed. In this case all critical parameters must be carefully measured to insure accurate simulation. Reference 4 describes methods of measuring FET parameters. Noncritical values may be taken from the specification sheet, if available, or estimated.

2. Nonlinear Element Parameters

The pinch-off voltage, V_P, and the drain saturation current, I_{DSS}, are two of the parameters required in the models presented here. While I_{DSS} is very easily measured it is difficult to measure V_P with much accuracy, since the transconductance and current become very small as V_P is approached. We can determine V_P much more accurately by measuring a different parameter. For the pinch-off region, the transconductance is given by equation 18,

$$g_m = \frac{2I_{DSS}}{-V_P}\left[1 - \frac{v_{GS}}{V_P}\right] . \qquad (18)$$

By evaluating g_m at $v_{GS} = 0$ where g_m is maximum,

$$g_{max} = \frac{2I_{DSS}}{-V_P} .$$

Then

$$V_P = -\frac{2I_{DSS}}{g_{max}} . \qquad (23)$$

Since g_{max} is easily determined at the same bias point as I_{DSS} they can be measured simultaneously. The circuit used in this study to measure these values is shown in figure 6. Table I lists parameters determined by this method for two types of FETs chosen for this study. Accuracy is

TABLE I

Parameter values for two types of field-effect transistors

FET Type	I_{DSS} (mA)	g_{max} (μmho)	V_P (volts)	C_{gs} (pf)	C_{dg} (pf)	C_{ds} (pf)
2N3819 (JFET)	4.1	4000	-2.05	8.	4.	4.
40468A (IGFET)	13.2	6010	-4.39	5.38	0.12	1.28

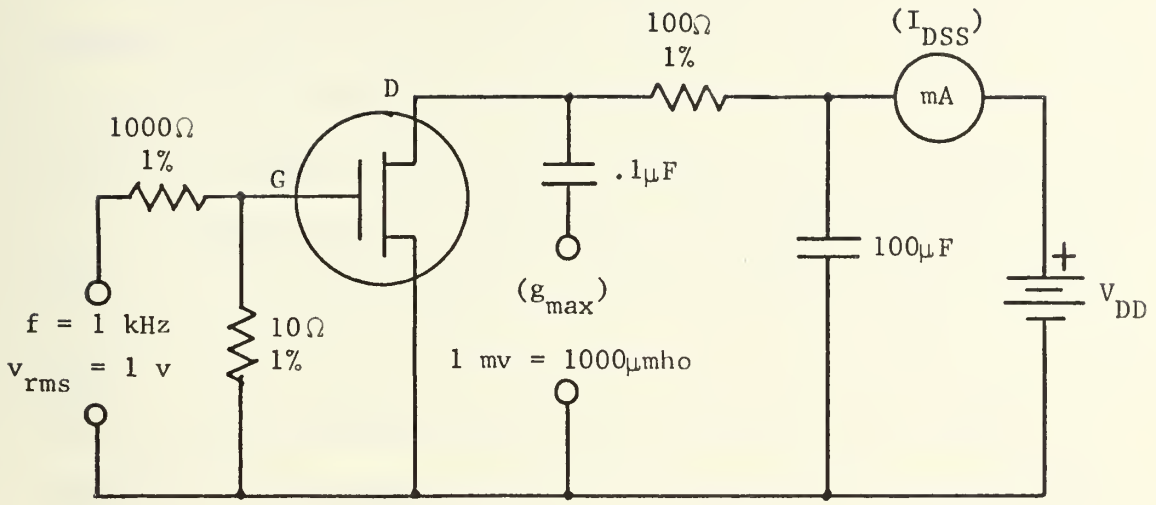


Figure 6. Circuit for simultaneous measurement of I_{DSS} and g_{max}.

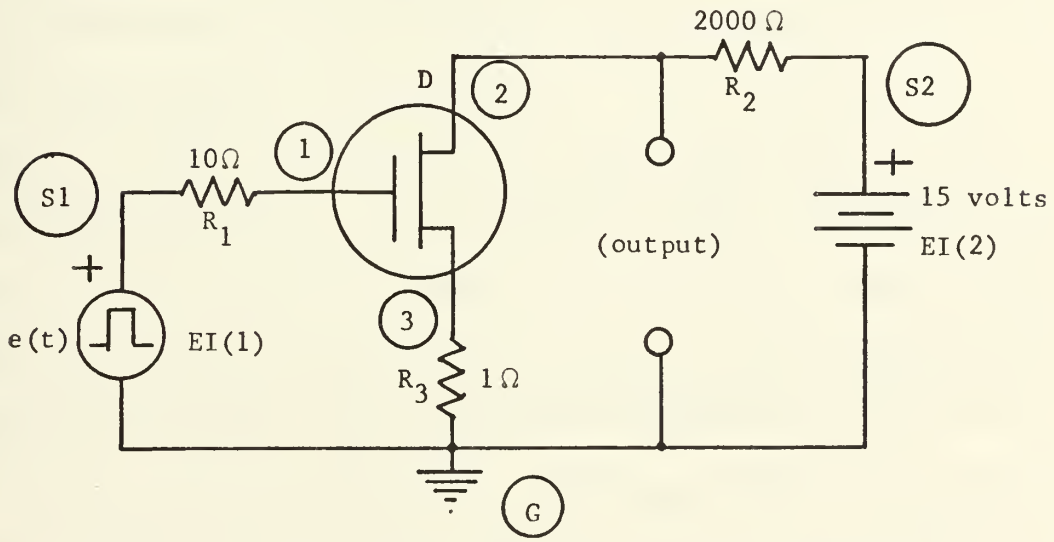


Figure 7. Pulse inverter circuit. Node numbers used in the TRAC program are encircled. EI(k) is the FORTRAN coding for the k^{th} grounded voltage source. The nodes G, S1, and S2 are not independent nodes and do not enter into the set of simultaneous equations solved by TRAC analysis.

indicated by the number of significant figures used. Results must be interpreted with caution since the computer program expresses numerical results to many more significant figures than can be justified on the basis of the model and accuracy of the empirically determined parameters.

In modelling the junction FET, a TRAC built-in diode model has been used. This model requires that the parameter I_{GSS} be supplied. I_{GSS} may be determined by shorting the drain to the source, applying a reverse bias, and measuring the source-to-gate current under this condition. If the FET is never to be operated in a forward-biased condition, this parameter is not critical since the current will be insignificant, and the value may be taken from the specification sheet.

3. Determination of Capacitance Values

The models presented in figure 5 have three capacitance values which must be determined: C_{gs}, C_{dg}, and C_{ds}. The TRAC diode model used in the JFET also requires a value for C_{d0}, the maximum at $v_{GS} = 0$ of the voltage-variable diode capacitance. This is the bias level at which C_{iss} and C_{rss} are measured. The input capacitance, C_{iss}, the output capacitance, C_{oss}, and the reverse-transfer capacitance, C_{rss}, were very small for the two FETs used in this study. While it would have been possible to measure these values, they were taken from the specification sheets. The capacitances required in the model can be determined from these parameters. Since C_{iss} is the input capacitance with the drain shorted to the source, $C_{iss} = C_{gs} + C_{dg}$. Similarily, $C_{oss} = C_{ds} + C_{dg}$ and $C_{rss} = C_{dg}$. These relationships can be solved for the required values:

$$C_{dg} = C_{rss}$$

$$C_{gs} = C_{iss} - C_{rss}$$

$$C_{ds} = C_{oss} - C_{rss}$$

Values determined for these capacitors are shown in table I. In the FET, C_{gs} is supplied to the diode model, which automatically varies gate capacitance with voltage.

B. MODEL PERFORMANCE

Large-signal dynamic models, while capable of simulating the operation of small-signal amplifiers and other small-signal circuits, are more importantly capable of simulating switching transients. For this reason the simple pulse-inverter circuit shown in figure 7 was chosen to demonstrate the ability of the proposed models to simulate device behavior accurately. This circuit was coded for TRAC analysis and was physically constructed with the same FETs which had been used in parameter determinations. Waveforms were observed and signal levels recorded to provide a basis for evaluation of model performance.

Figure 8 shows the junction FET model response to a 0.35-microsecond pulse with a rise time of 5 picoseconds. The input pulse level went from V_P to zero to turn on the device. Comparison of model transient response to actual transient response is summarized in table II.

The acutal device was pulsed by a Datapulse type-101 pulse generator which has a 5-nanosecond rise time. The voltages v_{GS} and v_{DS} were displayed on a Tektronix type-551 dual trace oscilloscope triggered by the pulse generator. A type 53/54K preamp having a rise

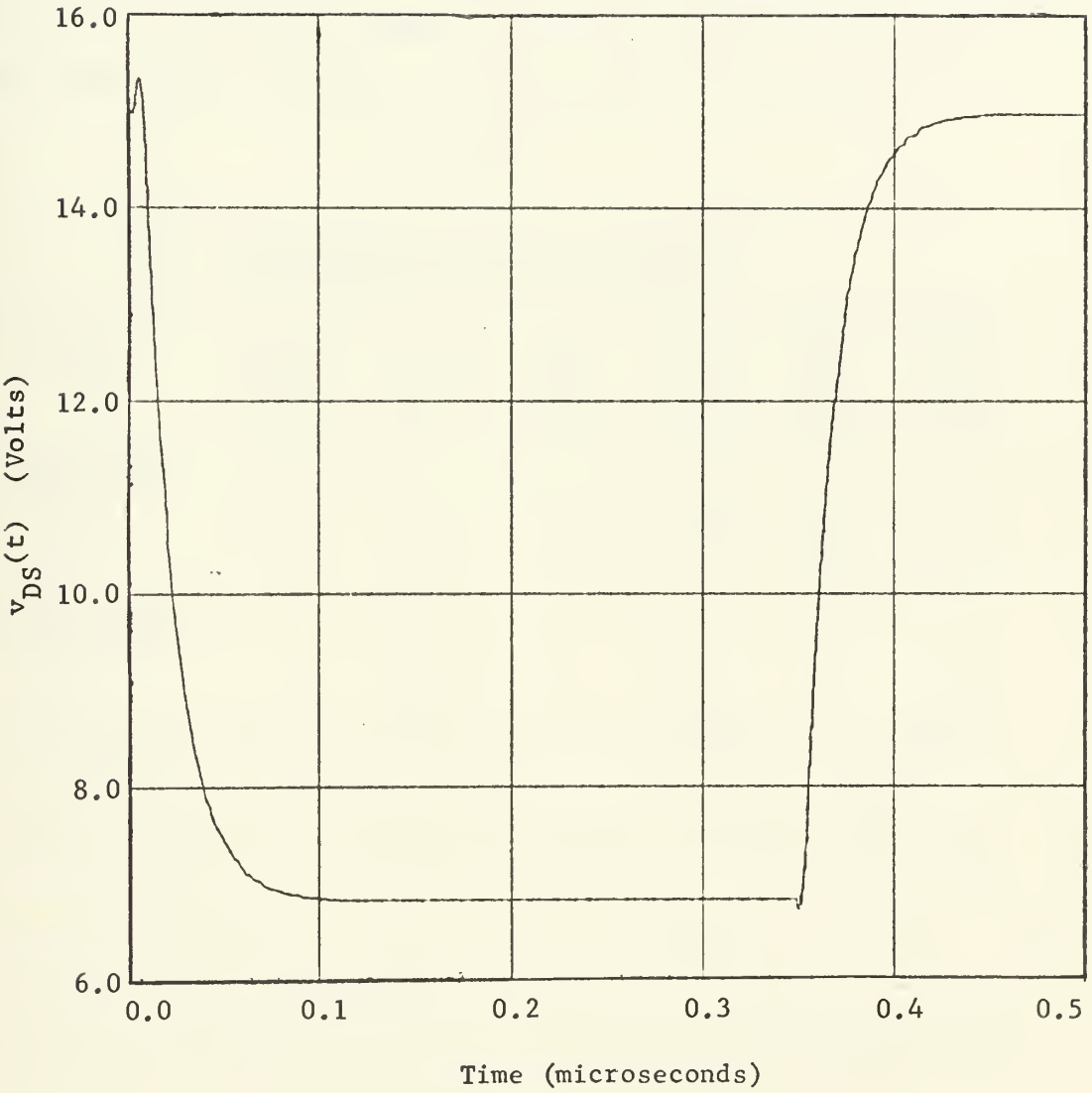


Figure 8. Junction FET model response to a 0.35 microsecond input pulse of a 5 nanosecond rise time.

time of 0.006 microseconds was installed. Measurements were made with compensated RF probes but no other attempt was made to reduce stray capacitance in the circuit.

The computer programming for the model of this circuit is included in Appendix A. Subroutine TRAEQ is called by TRAC to supply the required matrix terms for the nonlinear portion of the model.

TABLE II

Comparison of switching levels and transients for FET model and actual device

FET Type	v_{DS}(ON) (volts)	v_{DS}(OFF) (volts)	ON delay (μsec)	Rise Time (μsec)	OFF delay (μsec)	Fall Time (μsec)
2N3819 JFET						
actual	6.8	15.0	0.018	0.102	0.011	0.100
model	6.83	14.99	0.0135	0.055	0.005	0.075
40468A IGFET						
actual	1.8	15.0	0.016	0.020	0.005	0.070
model	1.40	14.79	0.0	0.006	0.0	0.005

Figure 9 shows the IGFET model response to a similar exitation. The input pulse level was changed to match V_P for the IGFET. Performance comparison with the actual circuit is included in table II. Rise time was much faster with this FET since it is a high-frequency type. Measurements were made with the same equipment described above. Subroutine TRAEQ was the same as that used for the JFET. The TRAC data deck was modified to enter data appropriate to the type 40468A parameters.

Table II shows that in most cases the compared values were reasonably well in agreement. The ON voltage of the IGFET was substantially

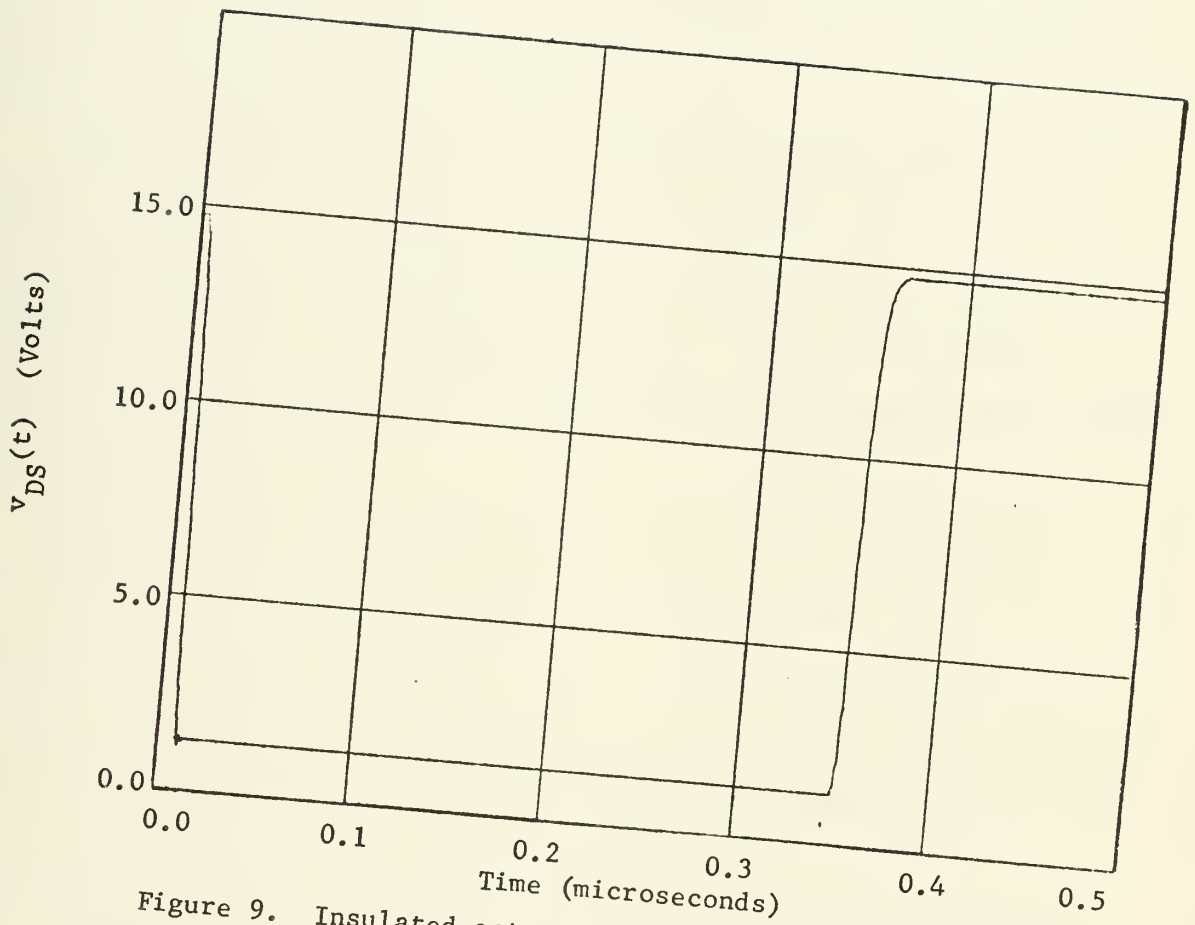


Figure 9. Insulated-gate FET model response to a 0.35 microsecond input pulse of 5 nanosecond rise time.

lower in the model than in the actual device. This was attributed to the determination of I_{DSS} and g_{max} by using a CW signal at zero gate bias which generated quite a lot of heat. This resulted in using a value for I_{DSS} in the model which was valid for a temperature higher than was actually present during the low-duty-cycle pulsed operation of the inverter circuit. Even so, the value obtained was well within the expected parameter spread for this device type.

Actual rise and fall times were consistantly greater than simulated values. This was to be expected since circuit stray capacitance was not included in the model circuit. Except when the FET is part of an integrated circuit, stray capacitance will be significant compared to device internal capacitances, and should be included where rise and fall times are critical.

The delay times in the JFET model response were due to the time constant associated with the charge storage capacitance which is included in the TRAC diode model. This resulted in a short spike which can be seen in figure 8 at the switch-on point. Actual circuit delay times were quite small. Delay times in the IGFET model response were zero since no delay was included in the model.

TRAC permits as many as 200 iterations before signaling nonconvergence of nonlinear models. Observation of intermediate results during the TRAC solution revealed that usually not more than two iterations were required to achieve convergence and quite often the initial solution was accepted.

V. CONCLUSIONS

A. GENERAL

The field-effect transistor models proposed here simulated actual device behavior quite well over the normal large-signal operating range associated with switching circuits. For a reasonably accurate simulation the parameters required for the model were few and easily determined. The models are fully compatable with TRAC, a very flexible network analysis program, and converged rapidly, as was expected, resulting in computational efficiency. These models lack a time-delay feature but otherwise have excellent transient behavior.

Emphasis was placed on empirical determination of parameters; however these might also be determined from the material characteristics and structural geometry of the device being modelled.

B. SUGGESTIONS FOR FURTHER STUDY

1. Simulation of Multiple-Device Circuits

While the circuit chosen to demonstrate the models was a single-device network, the matrix terms which were derived are applicable to any number of devices in the same network. The expressions were given in terms of the general gaté node, source node, and drain node. Where more than one FET is included in a circuit the appropriate network node numbers must be assigned for each terminal. Where leads from more than one FET are connected to the same set of nodes the more general expression for adding the k^{th} FET contribution is $H(P, Q) = H(P, Q) + H(P, Q)_k$. No coding problems should arise but convergence may be a problem in circuits with feedback and interaction between several device terminal voltages.

2. Dual-gate IGFET Simulation

Drain current in a dual-gate IGFET is a function of v_{DS} and the voltages on the two gates. An approximate analytical expression for this functional relationship must be obtained to implement pointwise linearization. One of the problems anticipated is that there is no simple division into operating regions as in the case of the single-gate IGFET. Since there are two independent gate electrodes there are several operating conditions possible at each point along the channel; furthermore, these conditions can exist simultaneously at different points in the same structure. A particular set of boundary conditions applies to the continuity equation for each possible combination of channel conditions.

3. Temperature Effects

I_{DSS}, V_P, and V_T are related to carrier mobility which is temperature dependent. TRAC includes temperature effects in its diode and bipolar junction transistor models and the temperature can be varied as a function of time and network variables by statements in the TRAEQ subroutine deck. Given expressions for parameter temperature dependence it should be simple to extend these models to include temperature effects.

4. Other Factors Affecting Model Accuracy

The models presented here assumed negligible output conductance in the pinch-off region. Further work is required to develop an approximate analytical expression for this conductance which can be linearized to provide a more accurate solution in the pinch-off region.

If a FET is to be operated outside of its normal range, it is necessary to include breakdown effects. It is possible that these

effects could be modelled using standard TRAC elements. The possibility of handling destructive breakdown by logical programming in the TRAEQ subroutine can be investigated.

In an actual device the active channel must be extended beyond the gate area to permit the source and drain contacts to be attached. Since the channel is lightly doped this adds significant bulk resistance to each of the terminals of the device. Further, there are small contact potentials which have been neglected. These and other extrinsic effects must be included for precision simulation.

```
C     TRAC CALLS THIS SUBROUTINE TO GET MATRIX TERMS FOR NONLINEAR MODELS

      SUBROUTINE TRAEQ (KK4)
      INTEGER CONP,COND,CONT
      REAL IDS
      REAL*8 AL(50),VER(12),AAAA(60),XXP(20),NPN,PNP,SYMB1,SYMB2,
     1TITLE(11),BCDT,BCDT1,A1,A2,A3,A8,DWORD,NDOF,STAR,O
      DIMENSION A(100),T(60),V1(120),V2(120),XP(700),TF(350),H(60,60),
     1NPP(60),NP1(10,2),VP(5000),E(19,16,2),EI(20)
     2,EP1(20),EP2(20),E2(19),TOO(19),JG(19),CT(11,2),PWTR(30),V(120),
     3    PWCR(30), QTAN(30,16), BCI(30), BCV(30), BCR(30), BEI(30), BEV
     4(30), BER(30), BCIP(30), PPIC(30), PPIC1(30), BEIP(30), PPIE(30),
     5PPIE1(30), QCR(30,7), DI(30), DV(30), DR(30), DIP(30), PPID(30), P
     6PID1(30),CONP(200,5),COND(30,5),CONT(30,5),NOP(4),VAL1(200),VAL2(2
     700), VAL3(200), BCUR(290), BCUR1(290), ST(19,2), VS(20,5),ZZ(3600)
      COMMON SI1,DM,O,BV,ARC,JSJ,TOL2,IBC,TOL1,IDC,E04,NAW,IAW,NCUT,KTOT
     1,ITOT,KTOT1,TOT2,NA,NA1,NV,NZ,NZ1,NT,NG,ND,ND1,NB,JJ,NBB,JJJ,N1B,N
     238,NVM,KE,JCAT,IEQ,TE,TE11,TI,TC,TC1,TC11,TOP,NBRAN,NCR,NTR,NCORE,
     3NBLOCK,NNNN1,TOLPL,TOLCR,ITOT1,ICP,IFGDTC,JVJ,JUJ,IPRINT,JV,NP,N2B
     4,NTPLP,IPX,IPLCON,ISTRK,SYMB1,SYMB2,ISYM3,ISYM4,BCDT,BCDT1,GRSP,RM
     5AG,TITLE,XP,TF,H,T,A,CONP,VS,V,V1,V2,CT,NPP,AAAA,NP1,VP,E,EI,EP1,E
     6P2,E2,TOO,JG,ST,QTAN,QCR,PWTR,PWCR,BCI,BCV,BCR,BCIP,PPIC,PPIC1,BEI
     7,BEV,BER,BEIP,PPIE,PPIE1,DI,DV,DR,DIP,PPID,PPID1,COND,CONT,NOP,VAL
     81,VAL2,VAL3,BCUR,BCUR1,DUMMY,AL
      EQUIVALENCE (H(1),ZZ(1)),(XP(1),XXP(1))
      GO TO (9000,9003,9002,9001),KK4
 9000 CONTINUE
C     PART 1 - MATRIX AND TIME FUNCTION EQ-S. AFTER THIS CARD
C     OPERATING REGION DETERMINATION
      IF((V(1)-V(3))/A(3).GE.1.0) GO TO 12
      IF(V(2).GE.V(1)-A(3)) GO TO 3
C     A(2)=IDSS  A(3)=VP  A(6)=DELTA FOR CONVERGENCE CRITERIA
C
C     TRIODE REGION LINEARIZATION
      VGS=V(1)-V(3)
      VDS=V(2)-V(3)
      GDS=(A(2)/(A(3))**2)*(2.*(VGS-A(3))-2.*VDS)
      IDS=(A(2)/(A(3))**2)*(2.*(VGS-A(3))*VDS-(VDS)**2)
C
C     MATRIX TERMS FOR TRICDE REGION
      H(2,2)=GDS
      H(2,3)=-GDS
      H(3,2)=-GDS
      H(3,3)=GDS
      T(2)=GDS*VDS-IDS
      T(3)=-GDS*VDS+IDS
      RETURN
```

```
C       PINCH-OFF REGION LINEARIZATION
    3   VGS=V(1)-V(3)
        VDS=V(2)-V(3)
        GM=(A(2)/(-A(3)))*(1.-VGS/A(3))
        IDS=A(2)*(1.-VGS/A(3))**2
C       PINCH-OFF REGION MATRIX TERMS
        H(2,1)=GM
        H(2,3)=-GM
        H(3,1)=-GM
        H(3,3)=GM
        T(2)=GM*VGS-IDS
        T(3)=-GM*VGS+IDS
   12   RETURN
C
 9003   ABC=0.0
C       CONVERGENCE TESTS
        VKIM=VGS-V(1)+V(3)
        VXEN=VDS-V(2)+V(3)
        IF(ABS(VKIM)-A(6))  9,9,6
    9   IF(ABS(VXEN)-A(6))  5,5,6
    5   ABC=-1.
        A(4)=ABC
        RETURN
    6   ABC=1.0
        A(4)=ABC
        RETURN
 9002   ARC=-1.0
C       PART 3 NOT REQUIRED
        RETURN
 9001   CONTINUE
C       PART 4 - AUXILIARY EQUATIONS
        V(4)=V(1)-V(3)
        V(5)=V(2)-V(3)
        RETURN
        END


C     THE FOLLOWING JCL CARDS WERE REQUIRED TO ACCESS TRAC IN NPGS 360/67 STORAGE
/*
//LINK.HLM DD DSNAME=SC231.TRAC,UNIT=2314,                              X
//         DISP=(OLD,KEEP),VOLUME=SER=LINDA
//LINK.SYSIN DD *
      INCLUDE HLM(TRAC)
/*
//GO.SYSIN DD *
```

```
C     THE FOLLOWING CARDS CONSTITUTE THE DATA DECK FOR THE 40468A IGFET MODEL

      S     G     GROUND   CURRENT  RENT SOURCE FLOATING VOLTAGE SVOLTAG*   0CC1C
E      RESISTANCE  INDUCCAPACINODE FNODE TES      PART PARAMETER   TORS  *   00020
 MORE THAN   NO.  BRANCHERPCR-CONNECTED BETWEEN  SOURCES OR PROGRAM WILL*   CCC30
 NOT PROCEED NODE NUMBERTOR     NOT CONVERG     SSERIES SHUNT VALUE 20   *   00040
 60    200                                                               *   0CC50
      TRAC PROGRAM AUTONETICS  HDL 4/68  REVISED 8/69, 4/70              *   0CC60
1. -05.1     .1    1. -2010.    .005  24.    *  +     3 10 10 42 38 81350200*   0CC70
      NONLINEAR MODEL OF RCA 40468A DEPLETION-TYPE SILICON IGFET (MOST)
           05           03           02           00           -1          02 1 SET 1
            1 1          25            0            0            2           0 2 SET 1
 VGS        4 VDS        5
   .0100E-06    .C049E-06    .0010E-06    .0200E-06    .005E-06   0.050E-06 1 SET 4
   .0100E-06     .349E-06    .0010E-06    .3700E-06    .005E-06   0.400E-06 2 SET 4
   .01C0E-06     .500E-06                                                    3 SET 4
                                                                             4 SET 4
300.         C.0132       -4.39        0.00        0.0100       0.005
           0                                                                 1 SET 9
           5             0                                                   1 SET 10
 -4.0                              -4.0          .0050E-06     0.0        .0100E-06
   0.0           C.350E-06          -4.0         0.355E-06
           1          -1                                                     1 SET 10
        15.0                                                                 2 SET 10
           0                                                                 1 SET 11
           3
S          1           1 10.0                                                2 SET 12
           3G          0  1.0                                               2 SET 12
S          2           2   2000.0
           3                                                                 1 SET 13
           1           2 .001200E-10   0.0                    .999999E+12
           1           3 .053800E-10   0.0                    .999999E+12
           2           3 .012800E-10   0.0                      .9900E+10
           0                                                                 1 SET 14
           0                                                                 1 SET 15
           0                                                                 1 SET 16
END OF FILE
```

```
C     THE FOLLOWING CARDS CONSTITUTE THE DATA DECK FOR THE 2N3819 JFET MODEL

      S     G     GROUND   CURRENT  RENT SOURCE FLOATING VOLTAGE SVOLTAG*  00010
E      RESISTANCE  INDUCCAPACINODE FNODE TES     PART PARAMETER   TORS  *  00020
 MORE THAN   NO.  BRANCHERROR-CONNECTED BETWEEN  SOURCES OR PROGRAM WILL*  00030
 NOT PROCEED NODE NUMBERTOR    NOT CONVERG     SSERIES SHUNT VALUE 20   *  00040
 60    200                                                              *  00050
      TRAC PROGRAM AUTONETICS  HDL 4/68  REVISED 8/69, 4/70             *  00060
1. -05.1    .1    1. -2010.   .005  24.   *  +    3 10 10 42 38 81350200*  00070
      NONLINEAR MODEL OF THE 2N3819 SILICON N-CHANNEL JFET IN ALL REGION
           05          03          02          00          -1          02
            1 1         25           0           0           2           0 2 SET 1
 VGS        4 VDS       5
   .0100E-06   .0049E-06   .0010E-06   .0200E-06   .005E-06   0.050E-06
   .0100E-06    .349E-06   .0010E-06   .3700E-06   .005E-06   0.400E-06
   .0100E-06    .500E-06

  300.      0.00410      -2.05      0.00000     0.01414     0.001       1 SET 5
           0                                                            1 SET 09
           5          0
   -2.00                  -2.00      .0050E-06     0.0       .0100E-06
   0.0          0.350E-06   -2.0      0.355E-06
           1          -1                                                RAT01360
        15.0                                                            RAT01370
           0
           3
S          1          1 10.0                                            RAT01400
           3G         0  1.0                                            RAT01420
S          2          2  2000.0
           2
           1          2    0.04E-10    0.0              100.0E+09
           2          3    0.04E-10    0.0              100.0E+09
           0
           1
           1          3                0.0
    2.00E-09    2.0        .99999E+14    8.00E-12    0.62    0.500000E-08
           0
END OF FILE
```

BIBLIOGRAPHY

1. Angelo, E. J. Jr., Electronics: BJTs, FETs, and Microcircuits, p. 109-131, McGraw-Hill, 1969.

2. International Business Machine Corp., 1620 Electronic Circuit Analysis Program User's Manual, IBM Technical Publications Department, White Plains, New York, 1965.

3. North American Rockwell Corp., Transient Radiation Analysis By Computer Program (TRAC) - Vol. I, User's Guide, by E. D. Johnson and others, June 1968.

4. The University of Texas Laboratories for Electronics and Related Science Research Report No. 33, Computer Models of the Field-effect Transistor, by B. D. Roberts and C. O. Harbourt, 19 April 1967.

5. Storm, H. F., "Field-effect Transistor(FET) Bibliography," IEEE Transactions on Electron Devices, v. ED-14, p. 710-717, October 1967.

6. Schlegel, E. S., "A Bibliography of Metal-Insulator-Semiconductor Studies," IEEE Transactions on Electron Devices, v. ED-14, p. 728-749, November 1967.

7. Schegel, E. S., "Additional Bibliography of Metal-Insulator-Semiconductor Studies," IEEE Transactions on Electron Devices, v. ED-15, p. 951-954, December 1968.

8. Long, D. M., "A Radiation Effects Large Signal Equivalent Circuit for MOS Transistors," IEEE Transactions on Nuclear Science, v. NS-14, p. 210-216, December 1967.

9. Sevin, L. J. Jr., Field-effect Transistors, p. 17-23, McGraw-Hill, 1956.

10. Middlebrook, R. D., "A Simple Derivation of Field-Effect Transistor Characteristics," Proceedings of the IEEE, v. 51, p. 1146-1147, August 1963.

11. North American Rockwell Corp., Transient Radiation Analysis by Computer Program (TRAC) - Vol. II, Theory and Flow Graphs, by E. D. Johnson and others, June 1968.

12. Stanford Electronics Laboratories Technical Report TR-5501-1, SEL-69-069, Computer Aided Analysis of Insulated Gate Field-effect Transistors, by M. B. Barron, November 1969.

INITIAL DISTRIBUTION LIST

		No. Copies
1.	Defense Documentation Center Cameron Station Alexandria, Virginia 22314	2
2.	Library, Code 0212 Naval Postgraduate School Monterey, California 93940	2
3.	Professor S. G. Chan, Code 52Cd Department of Electrical Engineering Naval Postgraduate School Monterey, California 93940	1
4.	LCDR Arthur D. RATHJEN, USN % Supervisor of Shipbuilding Conversion and Repair, USN Drawer T Mayport Naval Station Jacksonville, Florida 32228	1
5.	Professor S. R. Parker, Code 52Px Department of Electrical Engineering Naval Postgraduate School Monterey, California 93940	1

Security Classification

DOCUMENT CONTROL DATA - R & D

(Security classification of title, body of abstract and indexing annotation must be entered when the overall report is classified)

ORIGINATING ACTIVITY (Corporate author)	2a. REPORT SECURITY CLASSIFICATION
Naval Postgraduate School Monterey, California 93940	Unclassified
	2b. GROUP

REPORT TITLE

NONLINEAR COMPUTER MODELS OF FIELD-EFFECT TRANSISTORS

DESCRIPTIVE NOTES *(Type of report and inclusive dates)*

Master's Thesis; June 1970

AUTHOR(S) *(First name, middle initial, last name)*

LCDR Arthur D. RATHJEN, USN

REPORT DATE	7a. TOTAL NO. OF PAGES	7b. NO. OF REFS
June 1970	52	12

a. CONTRACT OR GRANT NO.	9a. ORIGINATOR'S REPORT NUMBER(S)
b. PROJECT NO.	
c.	9b. OTHER REPORT NO(S) *(Any other numbers that may be assigned this report)*
d.	

10. DISTRIBUTION STATEMENT

[redacted]

11. SUPPLEMENTARY NOTES	12. SPONSORING MILITARY ACTIVITY
	Naval Postgraduate School Monterey, California 93940

13. ABSTRACT

Whenever active devices are included in an electronic circuit that is to be analyzed by a computer, appropriate models for these devices must be developed. A lumped large-signal dynamic model of the field-effect transistor (FET) is presented and the procedure for pointwise linearization of this model is described. This linearized model is suitable for use with the TRAC (Transient Radiation Analysis by Computer program) network analysis program. Implementation of this model using TRAC coding was demonstrated by programming an example circuit for each of two basic types of field-effect transistor. The performance of the model in simulating a basic pulse invertor circuit was compared with actual device behavior. Suggestions for extension of this work are included.

DD FORM 1 NOV 68 1473 (PAGE 1)

S/N 0101-807-6811

Security Classification

A-31408

KEY WORDS	LINK A		LINK B		LINK C	
	ROLE	WT	ROLE	WT	ROLE	WT
Computer Aided Design						
Field-effect Transistor Models						
Electronic Circuit Analysis						
FET Models						